Data Sheet Revision for AD353X/R

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Data Sheet Specification Comparison

Previous Rev

SPECIFICATIONS

TIMING CHARACTERISTICS

All input signals are specified with rise time (t_R) = fall time (t_F) = 1ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{INL} + V_{INH})/2. VDD = 2.7V to 5.5V, 1.08V ≤ IOVDD ≤ 1.98V, and VREF = 2.5V. All specifications are T_J = −40°C to +125°C, unless otherwise noted.

Table 4. SPI Interface Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_1	SCLK cycle time	20			ns
		80[1]			

New Rev

SPECIFICATIONS

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